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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,229	01/22/2002	Terry M. Turpin	509622000700	7994

25227 7590 03/08/2007
MORRISON & FOERSTER LLP
1650 TYSONS BOULEVARD
SUITE 300
MCLEAN, VA 22102

EXAMINER	
BELLO, AGUSTIN	
ART UNIT	PAPER NUMBER
2613	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/051,229	TURPIN ET AL.	
	Examiner	Art Unit	
	Agustin Bello	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirasaki (U.S. Patent No. 6,185,040) in view of Miron (U.S. Patent No. 7,002,696).

Regarding claims 1, 3, 5, 9, 11, 13, Shirasaki teaches a transmitting system comprising: a processor (reference numeral 206 in Figure 16) to process at least one collimated input beam (e.g. output of collimator 322a in Figure 16) which has been modulated with a data signal (column 1 lines 55-57 and column 11 lines 21-22) to produce multiple time-delayed output taps (inherent delay caused by element 206 in Figure 16, also shown in Figure 7), the multiple time-delayed output taps being spatially distributed (column 4 lines 1-5), spatially distinct (as seen in Figure 7) and independently phase shifted (column 9 lines 46-47); an integration lens (reference numeral 322b in Figure 16) to receive the phase modulated output taps and to reintegrate the phase modulated output taps into a single encoded beam with a time series chip sequence, and an optical fiber (reference numeral 318 in Figure 16) to receive the integrated encoded beam from the integration lens and to transmit the integrated encoded beam. Shirasaki differs from the claimed invention in that Shirasaki fails to specifically teach that the processor is configured to maintain the collimation of the input beam so that the multiple time-delayed output taps maintain the collimation of the input beam. However, Miron, in the same field of transmitting systems,

teaches that this concept is well known in the art (Figure 2a). One skilled in the art would have been motivated to form the processor so that it is configured to maintain the collimation of the input beam so that the multiple time-delayed output taps maintain the collimation of the input beam in order to prevent beam interference. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to the processor is configured to form the processor so that it is configured to maintain the collimation of the input beam so that the multiple time-delayed output taps maintain the collimation of the input beam.

Regarding claims 2, 6, 7, 10, 12, 14, Shirasaki teaches a receiving system comprising: a processor (reference numeral 206 lower in Figure 16) to process the encoded collimated light taps received from a transmitter to produce multiple time-delayed output taps (inherent delay caused by element 206 in Figure 16, also shown in Figure 7), the multiple time- delayed output taps being spatially distributed (column 4 lines 1-5), spatially distinct (as seen in Figure 7) and independently phase shifted (column 9 lines 46-47); an integration lens (reference numeral 322b in Figure 16) to receive the phase-shifted output taps and to reintegrate the phase-shifted output taps into a single decoded beam; and a photo detector (column 11 lines 52-56) to receive the integrated decoded beam and to generate an output. Shirasaki differs from the claimed invention in that Shirasaki fails to specifically teach that the processor is configured to maintain the collimation of the input beam so that the multiple time-delayed output taps maintain the collimation of the input beam. However, Miron, in the same field of transmitting systems, teaches that this concept is well known in the art (Figure 2a). One skilled in the art would have been motivated to form the processor so that it is configured to maintain the collimation of the input beam so that the multiple time-delayed output taps maintain the collimation of the input

beam in order to prevent beam interference. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to the processor is configured to form the processor so that it is configured to maintain the collimation of the input beam so that the multiple time-delayed output taps maintain the collimation of the input beam.

Regarding claims 15-20, Shirasaki teaches that the modulation can be implemented in the spectral domain (e.g. each optical signal is shifted in phase with respect to each adjacent wavelength).

Regarding claims 21-26, Shirasaki's structure can be used as an optical equalizer.

Regarding claims 27-32, Shirasaki's structure can be used in a wide-band signal generation.

Regarding claims 4 and 8, Shirasaki differs from the claimed invention in that Shirasaki fails to specifically teach that the optical tapped delay device includes an etched plate having an etch depth sufficient to produce a desired phase shift though the time delayed output taps. However, etched plates for producing phase shifts in optical communication signals are well known in the art. One skilled in the art would have been motivated to employ an etched plate in the device of Shirasaki in order to produce a more pronounced phase shift in the signals output from the device. Moreover, Shirasaki's disclosure of a block structure that could have any suitable shape would have suggested an etched plate to one skilled in the art. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to employ an etched plate in the device of Shirasaki.

3. Claims 33-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirasaki in view of Miron and Ranalli (U.S. Patent No. 6,285,500).

Regarding claims 33, 36, Shirasaki teaches an optical tapped delay line device having a cavity to process at least one collimated input beam to produce multiple time delayed spatially distributed, spatially distinct (as seen in Figure 7) output taps in a linear array (as discussed above in the rejection of claim 1) and a two-dimensional photo detector array (reference numeral 118 in Figures 11 and 12) arranged to sample the interfering taps.

Shirasaki differs from the claimed invention in that Shirasaki fails to specifically teach a second input beam which projects at an angle to a plane of the optical tapped delay line linear array to interfere with each optical tapped delay line beam or an electronic amplifier to sample the photodetector array. However, Ranalli, in the same field of optics, teaches that it is well known to introduce a second beam to an optical system and allow the taps to interfere with a first set of delayed taps (see Figure 5). One skilled in the art would have been motivated to do so in order to reduce crosstalk and achieve greater optical performance (see abstract of Ranalli). Furthermore, electrical amplifiers for sampling photodetector arrays are well known in the art and readily available. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to introduce a second input beam which projects at an angle to a plane of the optical tapped delay line linear array to interfere with each optical tapped delay line beam as well as electrical amplifiers for sampling the photodetector array.

Shirasaki further differs from the claimed invention in that Shirasaki fails to specifically teach that the processor is configured to maintain the collimation of the input beam so that the multiple time-delayed output taps maintain the collimation of the input beam. However, Miron, in the same field of transmitting systems, teaches that this concept is well known in the art (Figure 2a). One skilled in the art would have been motivated to form the processor so that it is

configured to maintain the collimation of the input beam so that the multiple time-delayed output taps maintain the collimation of the input beam in order to prevent beam interference. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to the processor is configured to form the processor so that it is configured to maintain the collimation of the input beam so that the multiple time-delayed output taps maintain the collimation of the input beam.

Regarding claim 34, the combination of references teaches that the optical tapped delay line input beam is modulated with a data signal (as discussed in claim 1) and the second input beam is a coherent reference (inherent in the use of laser light in both systems).

Regarding claim 35, the combination of references teaches that the optical tapped delay line input beam is a coherent reference (inherent in the use of laser light in Shirasaki) and the second input beam is modulated with a data signal (column 7 lines 54-61 of Ranalli).

Regarding claims 37, the combination of references teaches that output beam to output beam delays propagate in a same direction (as seen in Figure 5 of Ranalli) in the optical tapped delay line device and the second optical tapped delay line device and an output of the receiving system is a correlation of the signals on the input taps.

Regarding claim 38, the combination of references differs from the claimed invention in that it fails to specifically teach that the output beam to output beam delays propagate in opposite directions in the optical tapped delay line device and the second optical tapped delay line device, and an output of the receiving system is a convolution of the signals on the input taps. However, one skilled in the art would clearly have recognized that it would have been possible to arrange the propagation of output beam delays in a number of different configurations, including one in

which the output beam delays propagate in opposite directions in the optical tapped delay line device and the second optical tapped delay line device, hence providing a convolution of the input signals. One skilled in the art would have been motivated to do so in order to further mix the first and second signals due to interference. Moreover, Ranalli clearly suggests convolution in the mixture of signals produced by the device. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to allow the output beam to output beam delays that propagate in opposite directions in the optical tapped delay line device and the second optical tapped delay line device, thereby producing an output of the receiving system which is a convolution of the signals on the input taps.

Response to Arguments

4. Applicant's arguments with respect to claims 1-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Agustin Bello whose telephone number is (571) 272-3026. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571)272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Agustin Bello
Primary Examiner
Art Unit 2613

AB